Solid-State Electronics 111 (2015) 67–75

Contents lists available at ScienceDirect

Solid-State Electronics

journal homepage: www.elsevier.com/locate/sse

Short channel amorphous In–Ga–Zn–O thin-film transistor arrays for ultra-high definition active matrix liquid crystal displays: Electrical properties and stability

Soo Chang Kim [a,b], Young Sun Kim [a], Eric Kai-Hsiang Yu [b], Jerzy Kanicki [b,*]

[a] YE Team, Samsung Display, Asan, Chungnam 336-741, South Korea
[b] Solid-State Laboratory, Electrical Engineering & Computer Science, University of Michigan, Ann Arbor, MI 48109, USA

ARTICLE INFO

Article history:
Received 17 November 2014
Received in revised form 18 April 2015
Accepted 6 May 2015
Available online 5 June 2015

Keywords:
In–Ga–Zn–O
Thin-film transistor
Active matrix liquid crystal display (AM-LCD)
Short channel effect
Tikhonov's regularization
AC bias-temperature stress stability (AC BTS)

ABSTRACT

The electrical properties and stability of ultra-high definition (UHD) amorphous In–Ga–Zn–O (a-IGZO) thin-film transistor (TFT) arrays with short channel (width/length = 12/3 μm) were examined. A-IGZO TFT arrays have a mobility of ~6 cm^2/V s, subthreshold swing (S.S.) of 0.34 V/decade, threshold voltage of 3.32 V, and drain current (I_d) on/off ratio of <10^9 with I_{off} below 10^{-13} A. Overall these devices showed slightly different electrical characteristics as compared to the long channel devices; non-saturation of output curve at high drain-to-source voltage (V_{ds}), negative shift of threshold voltage with increasing V_{ds}, and the mobility reduction at high gate voltage (V_{gs}) were observed. The second derivative method adopting Tikhonov's regularization theory is suggested for the robust threshold voltage extraction. The temperature dependency of γ-value was established after taking into consideration the impact of source/drain contact resistances. The AC bias-temperature stress was used to simulate the actual operation of active matrix liquid crystal displays (AM-LCDs). The threshold voltage shift had a dependency on the magnitude of drain bias stress, frequency, and duty cycle due to the impact ionization accelerated at high temperature. This study demonstrates that the short channel effects, source/drain contact resistances and impact ionization have to be taken into account during optimization of UHD AM-LCDs.

© 2015 Elsevier Ltd. All rights reserved.

1. Introduction

Oxide semiconductors such as an amorphous indium gallium zinc oxide (a-IGZO) have been intensively studied for past ten years especially for the application to next generation flat panel displays [1–3]. Superior characteristics of the a-IGZO thin film transistors (TFTs) as compared to the hydrogenated amorphous Si (a-Si:H) TFTs such as a high field effect mobility and transparency have increased their potential to become switching or driving transistors in next generation active matrix liquid crystal display (AM-LCD) or active matrix organic light emitting diode (AM-OLED), respectively. Today it has been already established that a-IGZO TFTs can be processed uniformly over large-size area at low temperature, and can use existing active-matrix arrays production infrastructure [4–6]. Recently, the high-end displays with the ultra-high definition (UHD > ~4000 × 2000 pixels), large-area (>70 in.), and high frame rate (>240 Hz) are being introduced to realize displays with more realistic visual images [7]. To fabricate such displays, the dimension of TFTs, such as channel length and width, needs to be reduced to keep a high transmittance of pixel electrodes without any decrease of pixel aperture ratio and carrier mobility. Prior studies have focused on the electrical performance or electrical stability of TFTs with the relatively large channel width W (>100 μm) and length L (>10 μm) to avoid the short channel and source/drain contact effects. Moreover, all reports published so far on a-IGZO TFTs have focused on a single TFT structures [8–12]. To our best knowledge, there is no report in open literature on electrical characteristics of the a-IGZO TFT arrays with a short channel length used in the UHD AM-LCDs. It is important to notice that the exact understanding of the fundamental electrical properties of the a-IGZO TFT arrays with a UHD resolution is required to objectively compare the electrical behaviors of the devices manufactured under different conditions. Recent studies of a-IGZO electrical bias-temperature stability (BTS) have employed a pulsed AC gate and/or drain bias simultaneously to reflect the typical driving scheme in AM-LCDs [13–18]. However, the unipolar pulsed gate stress (*e.g.* 0 V to positive or negative to 0 V pulse) has been often used with the source/drain grounded. Also the duty cycle, which is defined as the ratio of turn-on time

* Corresponding author. Tel.: +1 734 936 0964; fax: +1 734 615 2843.
E-mail address: kanicki@umich.edu (J. Kanicki).

http://dx.doi.org/10.1016/j.sse.2015.05.002
0038-1101/© 2015 Elsevier Ltd. All rights reserved.

(t_{on}) to frame time (t_{frame}), was too large (25–75%) as compared with the typical duty cycle used in AM-LCDs ranging from 0.05% to 1% depending on the display resolution and refresh rate.

In this work, we examined in details the electrical characteristics of the a-IGZO TFT arrays used in the ultra-high definition displays panel with relatively short channel dimension (W = 12 μm, L = 3 μm) and we studied the bias-temperature stability using the AC pulsed gate and drain bias-temperature stress to simulate the actual operation of the AM-LCDs.

2. Experimental

A-IGZO TFT arrays were fabricated in a well-controlled manufacturing line on the glass substrate following the similar process described in [5,7]. The TFT has a back channel etched (BCE) inverted staggered bottom-gate structure. The active layers were deposited by conventional sputtering technique with optimized conditions so that it has In:Ga:Zn = 1:1:1 non-stoichiometric composition. The array is composed of 100 same-structured TFTs which are connected in parallel as shown in Fig. 1. The measured total drain current (I_d) was divided by 100 to obtain the average I_d representing one single TFT. We verified independently that the average TFT characteristic is very similar to single TFT measured separately. In manufacturing environment, it is very important to investigate the TFT arrays rather than single TFT properties for monitoring the uniformity and quality during the manufacturing process. The channel width and length of individual TFT is about 12 μm and 3 μm, respectively.

The electrical characteristics of a-IGZO TFT arrays were measured at 0.2 V steps using an Agilent B1500A semiconductor parameter analyzer in ambient air and dark conditions. The sample temperature was regulated by a heated chuck of the probe station. The measurements were repeated several times to acquire reproducible data. The B1500A and a HP 8114A pulse generator are connected to an HP E5250A switching matrix to measure the AC bias-temperature stress (AC BTS) stability [18]. An Agilent EasyExpert software routine automatically switches the E5250A between the HP 8114A for AC stressing and the B1500A for device measurement. Fig. 2 shows the AC gate pulse ranging from V_{GL} = −5 V to V_{GH} = +15 V and DC V_{ds} (0/5/10 V) voltage used in this study. Since the drain voltage continuously fluctuates (*e.g.* from 0 V to 10 V with the center being common voltage) to supply the appropriate voltage corresponding the gray scale level, it is reasonable to set the drain-to-source voltage (V_{ds}) at a constant DC voltage during AC BTS. The accumulated stress time is defined as the total time a gate bias (negative or positive) is applied to the gate electrode. The device stressing is interrupted at predetermined time intervals to measure the TFT transfer characteristics at stress temperature (T_{st}) 70 °C.

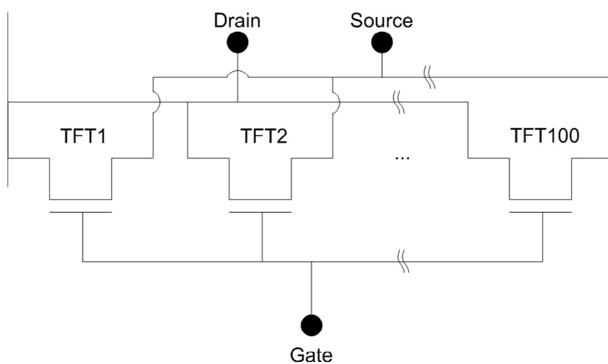


Fig. 1. Schematic diagram of the 100-TFT-array used in this study.

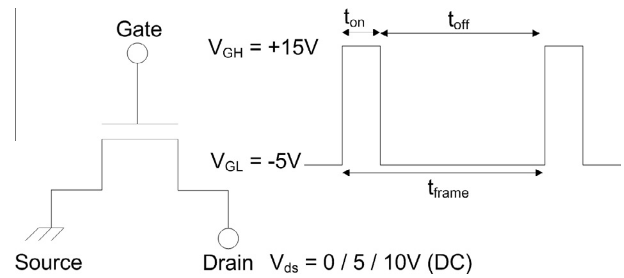
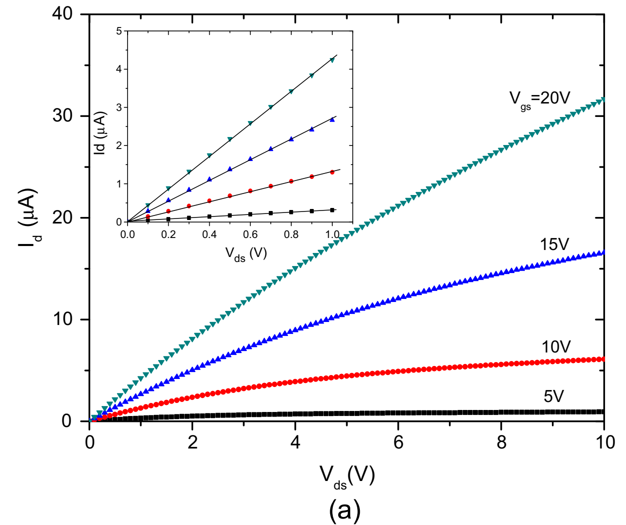


Fig. 2. Schematic diagram of the pulsed gate bias and DC drain bias stress conditions used in this investigation.



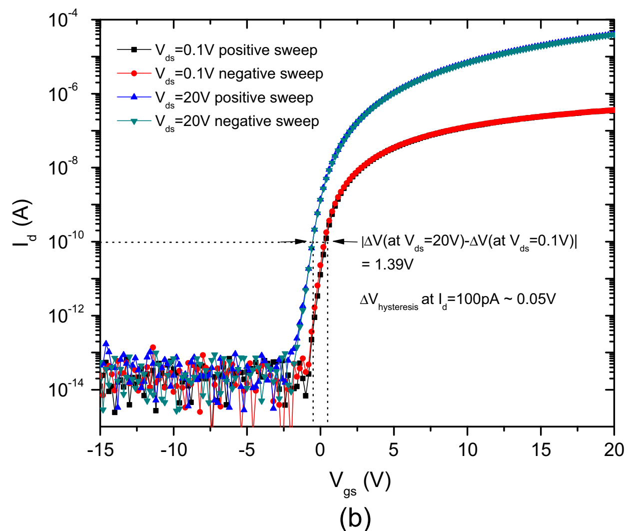


Fig. 3. (a) The average I_d–V_{ds} output and (b) average I_d–V_{gs} transfer TFT characteristics are shown. The (a) inset shows no current crowding is observed close to the origin of the output plot. The hysteresis between positive and negative sweep is small (about 0.05 V) in the subthreshold region.

3. Results and discussion

3.1. TFT electrical characteristics

Fig. 3(a) shows typical averaged output curve at different gate bias voltage (V_{gs}). The inset shows no significant current crowding at low drain-to-source voltage (V_{ds}) close to the origin of the output

curve indicating that a good contact was formed between the Cu-based source/drain electrodes and a-IGZO. However, the drain current (I_d) at high V_{ds} does not saturate and the non-saturation becomes more significant at higher gate biases. This effect is commonly observed in a-Si:H TFT [19] and polysilicon TFT [20] as well as in a single a-IGZO TFT [8–11] (normally for $L < 4$ μm) when the channel length is reduced. This non-saturation is associated with the channel length modulation which accounts for the I_d increase resulted from the shrinking channel length with the application of V_{ds} in excess of the saturation drain-to-source voltage (V_{dsat}). The degree of the channel length modulation is expressed by the channel length modulation parameter λ in the saturation region as follows [21]:

$$I_d = I_{dsat}[1 + \lambda(V_{ds} - V_{dsat})], \tag{1}$$

where V_{dsat} and I_{dsat} are the V_{ds} and I_d when the slope of output curve $\left(\frac{\partial I_d}{\partial V_{ds}}\Big|_{V_{gs}=const.}\right)$ is first matched with the experimental data. The parameter λ values range from 0.037 V^{-1} at V_{gs} = 5 V to 0.058 V^{-1} at V_{gs} = 20 V. It is speculated that the channel length modulation effect increases with increasing V_{gs} for TFTs with short channels. Fig. 3(b) shows a representative averaged transfer curve at V_{ds} of 0.1 V and 20 V. The hysteresis between positive and negative sweep is small (about 0.05 V) in the subthreshold region. Negligible hysteresis indicates that very small number of electrons were trapped at or near the gate dielectric (a-SiN_x/a-SiO_x bilayer)/a-IGZO interface or within the a-IGZO active channel bulk. The on/off current ratio (I_{on}/I_{off}) is over 10^9 with I_{off} below 10^{-13} A. This low leakage current will prevent the voltage of the pixel capacitor from decreasing during the TFT off-state and during changing of the display's grayscale levels resulting in reduced power dissipation [3]. In general, the carrier field-effect mobility (μ) and TFT threshold voltage (V_{th}) are extracted from the standard MOSFET I_d–V_{gs} equation in the linear region (V_{ds} = 0.1 V) or/and saturation region (V_{ds} = 20 V) [22]:

$$I_{d(lin)} = \mu C_{ox}\frac{W}{L}(V_{gs} - V_{th})V_{ds}, \tag{2a}$$

$$I_{d(sat)} = \mu C_{ox}\frac{W}{2L}(V_{gs} - V_{th})^2, \tag{2b}$$

where C_{ox} is the gate insulator capacitance per unit area, W and L are TFT channel width and length, respectively. As Fig. 4(a) shows the 10–90% linear method used for extraction of the field-effect mobility and threshold voltage, considerable deviation between experimental and fitted curves can be observed. Since the carrier field-effect mobility (μ) extracted by the 10–90% linear method can be considered as average value, the incremental field-effect mobility (μ_{cal}) corresponding to specific V_{gs} should also be evaluated:

$$\mu_{cal} = \left(\frac{\partial I_d}{\partial V_{gs}}\right)\frac{L}{WC_{ox}V_{ds}}. \tag{3}$$

As shown in Fig. 4(b) and (c), μ_{cal} of a-IGZO TFT arrays depends on V_{gs} and temperature. As the temperature increases, a larger number of electrons that are thermally activated from the localized trap sites into the conduction band will contribute to a free carriers resulting in a higher mobility and smaller threshold voltage, Fig. 7 [23].

Another important TFT parameter is the subthreshold swing (S.S.) that was extracted as the average of three values nearest the maximum value in the subthreshold region using the following equation:

$$S.S. = \left\{\frac{d\log(I_d)}{dV_{gs}}\right\}^{-1}. \tag{4}$$

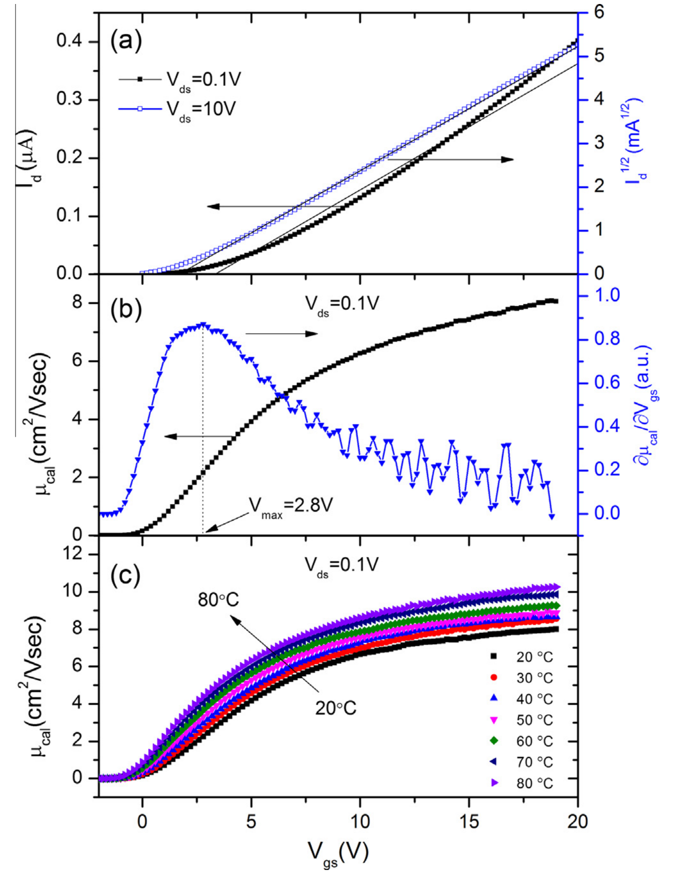


Fig. 4. (a) The average I_d–V_{gs} transfer TFT characteristics in the linear and saturation region of operation are shown. Solid lines are the linear fits using 10–90% linear method. (b) The μ_{cal} and its derivatives, extracted from the average transfer characteristics, as a function of gate bias are shown. (c) The μ_{cal} variation with the gate-to-source bias with different temperatures ranging from 20 °C to 80 °C is shown.

Table 1
Extracted a-IGZO TFT electrical properties for different V_{ds} using 10–90% linear method.

V_{ds} (V)	μ (cm^2/V s)	V_{th} (V)	S.S. (V/dec)	I_{on}/I_{off} ratio
0.1	5.96	3.32	0.34	<10^9
20	6.25	1.93	0.38	<10^9

The extracted parameters from the transfer curve in the linear and saturation regions are listed in Table 1.

From experimental data, compared to the long channel a-IGZO TFT, we observe that the negative shift of threshold voltage between linear (V_{ds} = 0.1 V) and saturation regime (V_{ds} = 20 V) is relatively large (1.39 V), Fig. 3(b). This shift can be understood by a charge sharing model and a drain induced potential barrier lowering (DIBL), in general, observed in a short channel MOSFETs [24]. The channel charges near the source/drain contacts are controlled by the electric field originating not only from the gate, but also from the source/drain electrodes. As a consequence, the portion of charges directly controlled by gate is reduced resulting in the V_{th} lowering at high V_{ds}. The DIBL is 69.9 mV/V, and can be calculated by [25]

$$DIBL = \left|\frac{V_{th}|_{V_{ds(sat)}} - V_{th}|_{V_{ds(lin)}}}{V_{ds(sat)} - V_{ds(lin)}}\right|. \tag{5}$$

Obtained DIBL value is comparable to value of the a-IGZO TFTs with $L < 4\ \mu m$ as shown by Baek et al. [25].

Expected I_{off} ($I_{off}/W \sim 10^{-15}$ A/μm) change with V_{ds} cannot be observed in our experiments since measured I_{off} is limited by experimental setup.

In Fig. 4(a), the linear region I_d–V_{gs} curve shows the non-linear behavior with V_{gs}. Fitting of the experimental data to Eq. (2a) is rather difficult and it will result in overestimation of V_{th}. Hence, the determination of V_{th} and mobility using the 10–90% linear method is not reliable for short channel TFT having non-linear I_d–V_{gs} characteristics. Other methods for threshold voltage extraction must be considered. One of possible methods is the transconduction change method. It is well known that only the transconductance change method can exclude the effects of the interface state, the mobility degradation, and the parasitic resistance, and can approach the physically meaningful threshold voltage [26–28]. In former studies [26–28], the transconductance change method defined the threshold voltage as the V_{gs} at which the second derivative of I_d to V_{gs} ($\partial^2 I_d/\partial V_{gs}^2$) is a maximum. Fig. 4(b) shows the determination of threshold voltage by the second derivative method ($V_{th} \approx 2.8$ V). Since the second-order differentiation tends to be very noisy and obtained results can vary with the measurement conditions, we suggest extracting more stable threshold voltage using the Tikhonov's regularization theory [29]. Tikhonov's regularization is useful to obtain meaningful solution estimates even for ill-conditioned measurements.

$$g(V) = \{A_h^T A_h + \alpha(B^T B + C^T C)\}^{-1} A_h^T f_\lambda, \tag{6}$$

where $g(V)$, V, f_λ, α, A_h, B_h, and C_h are the second derivative extracted by the regularization, V_{gs}, measured I_d, regularization parameter, the matrix representing the second order differentiation, the identity matrix, and the matrix representing the first order differentiation, respectively. The optimum regularization parameter α^* is defined as

$$dis|_{\alpha=\alpha^*} = \min\left(\int |A_h g - f_\lambda|^2 dV - \lambda^2\right), \tag{7}$$

where λ is discrepancy value of which variation had no effect on the results (not shown). Fig. 5(b) shows the second derivative profile extracted with the regularization parameter obtained in Fig. 5(a). In case of $\alpha = 0$, it gives us very noisy variation, preventing threshold voltage extraction. Once α is optimized ($\alpha = \alpha^*$), the noises are suppressed, resulting from the subthreshold region, and smooth curve is obtained enabling robust threshold voltage determination. It should be recognized that any variation in V_{th} extraction will impact the calculation of other TFT parameters such as gamma (γ) and K [30] values included in following equations:

$$\mu_{cal} = \left(\frac{\partial I_d}{\partial V_{gs}}\right)\frac{L}{WC_{ox}V_{ds}} = K\gamma(V_{gs} - V_{th})^{\gamma-1}. \tag{8}$$

$$I_d = KC_{ox}\frac{W}{L}(V_{gs} - V_{th})^{\gamma}V_{ds}. \tag{9}$$

The γ and K can be extracted from the linear fit of the log–log plot of μ_{cal} as a function of the effective gate voltage ($V_{gs} - V_{th}$) in Eq. (8). In other words, γ is obtained from the slope, ($\gamma - 1$), and K is calculated from the intercept when using the following equation:

$$\log(\mu_{cal}) = \log(K\gamma) + (\gamma - 1)\log(V_{gs} - V_{th}). \tag{10}$$

Fung et al. suggested the current ratio method to extract the V_{th} and γ at the same time using the Eq. (9) [30]. The V_{th} and γ are determined by selecting the best linear fit to the logarithm of following drain current ratio with minimum root mean square (RMS) error:

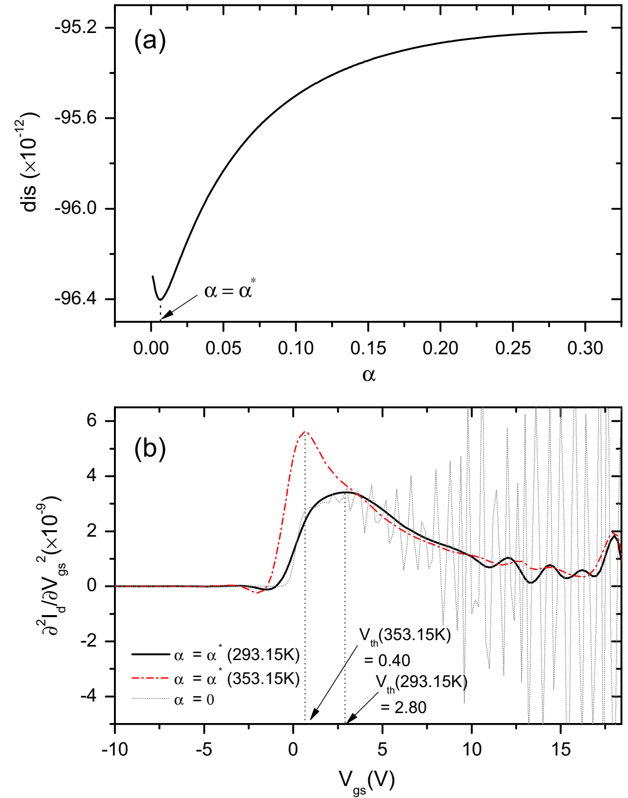


Fig. 5. Threshold voltage extraction using Tikhonov's regularization is shown. (a) Determination of the regularization parameter α, and (b) $\partial^2 I_d/\partial V_{gs}^2$ profiles extracted with optimum regularization parameter $\alpha = \alpha^*$ and $\alpha = 0$. Extracted V_{th} for two temperatures are shown.

$$\log\left(\frac{I_d}{I_0}\right) = \gamma\log\left(\frac{V_{gs} - V_{th}}{V_0 - V_{th}}\right), \tag{11}$$

where I_0 is the reference drain current at $V_{gs} = V_0$ and chosen to be much larger than the subthreshold current. Fig. 6 shows the extraction of V_{th} and γ at 20 °C using the current ratio method. It should be stated that this procedure is rather complicated since the least square fitting over a number of estimated V_{th} values have to be repeated to reach minimum RMS error. Also, when the threshold voltage shift with the temperature is close to or within the measurement resolution (0.2 V in this study), it can be difficult to extract the exact V_{th}.

Fig. 7 shows the evolution of threshold voltages with temperature extracted with four different methods, which are: (1) 10–90% linear method; (2) second derivative method adopting Tikhonov's regularization; (3) current ratio method; and (4) constant I_d (10^{-10} A) method. The second derivative method before and after adopting Tikhonov's regularization provided similar V_{th} results (not shown). The threshold voltage extracted by the second derivative method has expected non-linear dependence on temperature [31].

Fig. 8(a) compares the I_d fitting results with γ and K values extracted using four different threshold voltage extraction methods. Overall both current ratio and constant I_d methods do not provide satisfactory results. They fit relatively well the experimental data at low (~5 V) and high V_{gs} (18 V~) but showed the largest deviation at the intermediate V_{gs} (8–15 V). The 10–90% linear method results in I_d shift to the right as compared to the second derivative method adopting Tikhonov's regularization. The root mean square (RMS) error of the second derivative method for above threshold and intermediate V_{gs} range is the smallest of four

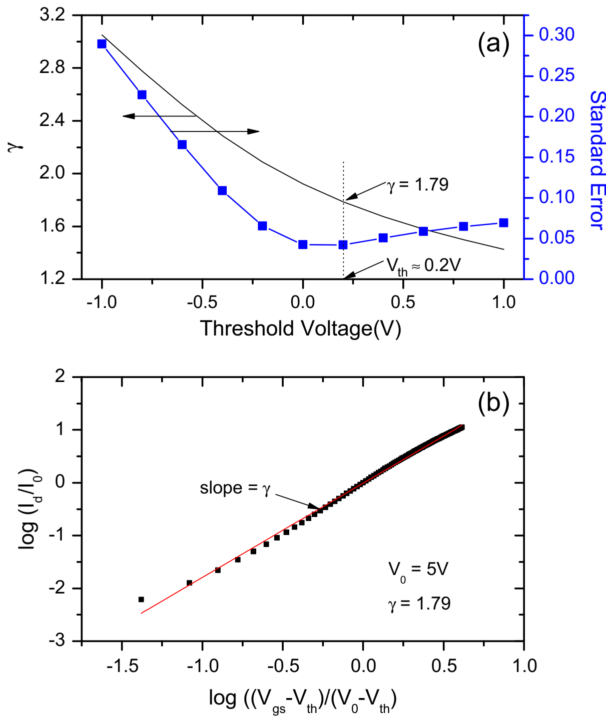


Fig. 6. Current ratio method for threshold voltage extraction at 20 °C is shown. (a) variation of γ and standard error of the linear fit as a function of V_{th}, and (b) linear fitting at V_{th} with minimum error are shown.

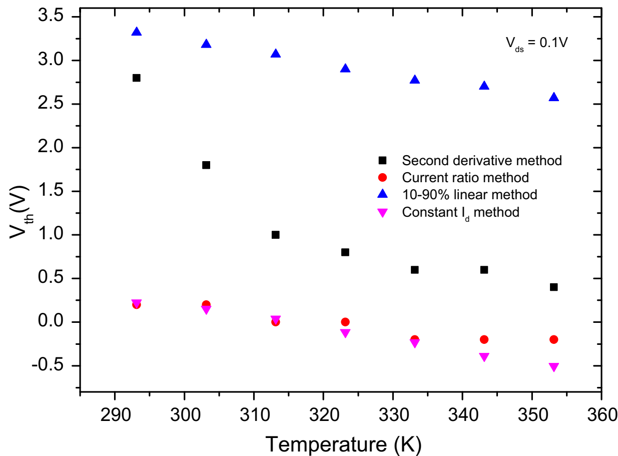


Fig. 7. Evolution of the threshold voltages with the temperature extracted with four different methods is shown.

methods considered in this study, as shown in Table 2. From our results, we concluded that the second derivative method is most suitable for extracting the threshold voltage of the a-IGZO TFT arrays. Still, the observed parallel shift (ΔV_{gs}) to the right needs

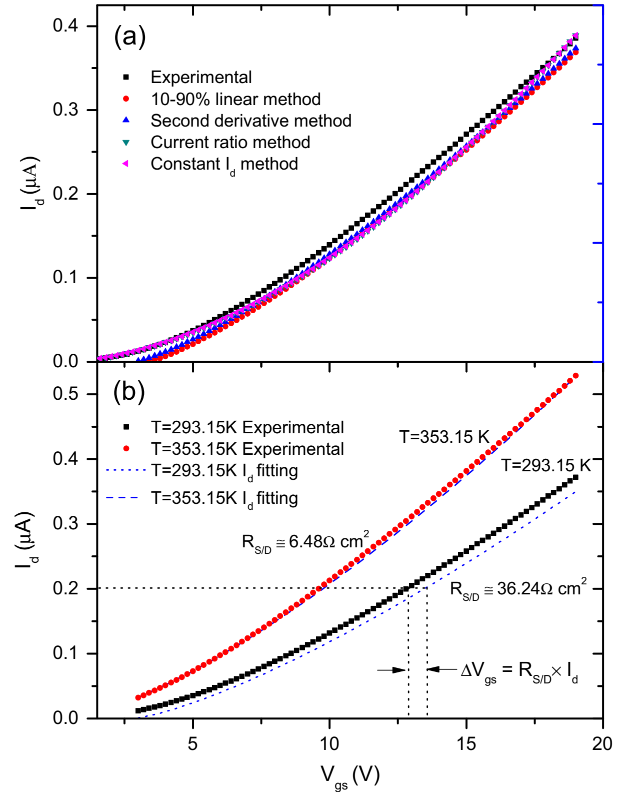


Fig. 8. (a) Comparison of the I_d fitting results above threshold region for γ and K values extracted using different threshold voltage extraction methods and (b) contact resistance estimated from the difference between the experimental I_d data and the fitted values with the threshold voltage extracted using the second derivative based on Tikhonov's regularization theory.

to be explained. This difference between calculated and experimental data becomes smaller at higher temperatures as shown in Fig. 8(b). We propose to explain this shift by the reduction of effective gate voltage ($V_{gs} - \Delta V_{gs}$) due to source/drain contact resistances ($R_{S/D}$), decreasing with the increasing temperature. Assuming that the difference between the fitting curves and experimental data is associated with the source/drain contact resistances ($\Delta V_{gs} = R_{S/D} \times I_d$), the $R_{S/D}$ decreases from 36.24 Ω cm^2 to 6.48 Ω cm^2 when the temperature increases from 20 °C to 80 °C. It can be speculated that for the a-IGZO TFT arrays, the contact resistance decreases with the increasing temperature as it was the case for a-Si:H TFT [32]. It is noted that as the V_{gs} increases, ΔV_{gs} increases slightly ($\Delta(\Delta V_{gs})$ ~0.18 V at 20 °C) since I_d is V_{gs} dependent ($\Delta V_{gs} \propto I_d \propto V_{gs}$). At high temperature (80 °C), ΔV_{gs} change with the V_{gs} decreases below 0.10 V. To simplify the I_d and mobility fitting, constant $R_{S/D}$ and effective gate voltage reduction ΔV_{gs} at I_d = 0.2 μA were used. Fig. 9(a) and (b), respectively, show the I_d and mobility fitted with γ and K extracted by taking the constant effective gate voltage reduction (about 1.4 V at 20 °C) into account. The I_d fitting results are not perfect and the deviation of mobility at high V_{gs} is relatively large. This deviation

Table 2
Root mean square errors between experimental data and the results fitted using the γ and K values obtained with four different V_{th} extraction methods.

Method	RMS (10^{-7}) (above threshold)	RMS (10^{-7}) (8 V < V_{gs} < 15 V)
10–90% linear method (Fig. 4(a))	1.483	1.011
Second derivative method using Tikhonov's regularization (Fig. 5)	1.070	0.749
Current ratio method (Fig. 6)	1.100	0.997
Constant I_d method (10^{-10} A) (Fig. 3(b))	1.074	0.972

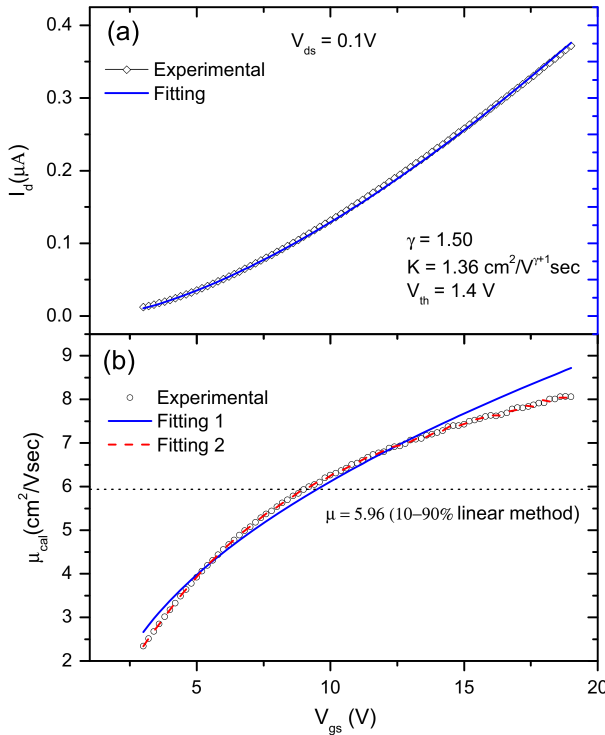


Fig. 9. The fitting of (a) I_d and (b) μ_{cal} with the extracted γ, K values for above threshold voltage region. Fitting 1 is calculated using only one γ and K value and fitting 2 takes into consideration the impact of the source/drain contact resistances for each V_{gs}.

comes from the mobility reduction caused by the source/drain contact resistances at high V_{gs} [9]:

$$\mu_{FE} \approx \mu_0 \frac{1}{1 + \mu_0 \frac{W}{L} C_{ox} R_{S/D}(V_{gs} - V_{th})}, \tag{12}$$

where μ_0 is the intrinsic mobility of the a-IGZO material. We would like to indicate that it is not possible to fit perfectly the mobility with single γ and K obtained using the least square method of Eq. (8) without taking into consideration the impact of the source/drain contact resistances. The impact of this contact resistance will change with the gate bias. Fitting 2 in Fig. 9(b) shows plot for which the source/drain contact impact with the gate bias was taken into consideration; this fitting corresponds well to experimental data.

Fig. 10 shows the evolution of threshold voltages extracted by the second derivative method adopting Tikhonov's regularization theory and γ value with increasing temperature after considering the impact of the source/drain contact resistances. The γ tends to decrease as the temperature increases as it would be expected from previous studies. But, the γ variation within investigated temperature range is relatively small range (0.1). The γ can be described by $2(T_G/T) - 1$ (a-Si:H TFT [33]) or by $T_\gamma/T + \gamma_0$ (a-IGZO TFT [34]); where T_G and T_γ are the characteristic temperature and γ_0 is a fitting parameter. Characteristic temperature is associated with the density of states (DOS) of conduction band tail. The T_γ and γ_0 can be extracted from the linear fit of γ as a function of the reciprocal temperature (T_γ = 150 K, γ_0 = 1.01). Extracted T_γ value indicates a low density of conduction band tail states and is in agreement with Abe et al.'s results [34]. From our results, we can conclude that the dependency of the effective gate voltage reduction in short channel device needs to be taken into account while extracting V_{th} and γ.

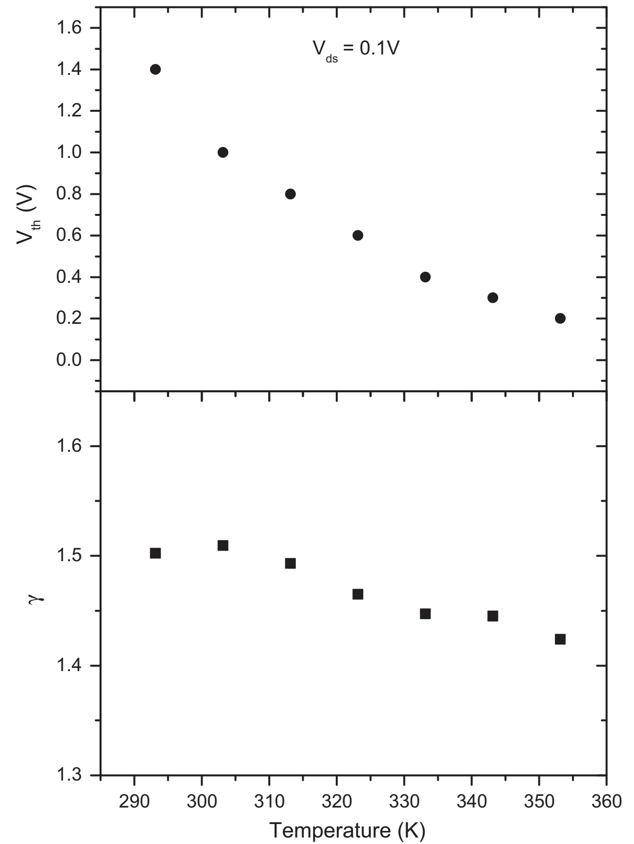


Fig. 10. Evolution of (a) threshold voltages extracted by the second derivative method adopting Tikhonov's regularization theory and (b) γ-value with the temperature after considering the impact of the source/drain contact resistances.

3.2. AC bias-temperature stress stability

Fig. 11(a) and (b) shows the representative evolution of the average TFT transfer curves with the stress time at stress temperature (T_{st}) of 20 °C and 70 °C, respectively, under the condition of pulsed V_{gs} = −5 V to +15 V, f = 240 Hz, V_{ds} = 10 V, and duty cycle = 0.046%. The transfer curve at 70 °C shifts to the negative direction more significantly than that at 20 °C, especially in the subthreshold region. In this section, for simplicity and to be consistent with other BTS studies, we define the threshold voltage (V_{th}) as the V_{gs} that induces a drain current (I_d) of 10^{-10} A, *e.g.* constant I_d method is used for V_{th} extraction. The carrier mobility change with AC BTS is negligible (within 3%) within investigated stress temperature. The subthreshold swing changed from 0.58 V/dec to 0.64 V/dec at 20 °C and from 0.56 V/dec to 0.75 V/dec at 70 °C during AC BTS indicating very negligible thermally accelerated defect generation in the bulk and/or interface between a-IGZO and gate a-SiN_x/a-SiO_x dielectric. It was found in Fig. 11(c) that the transfer characteristics can be recovered to its initial state when array is kept unstressed for an extended period of time at room temperature. This recovery can be accelerated by heating. In general, this behavior can be associated with the charge trapping at the interface between channel and gate dielectric; thermally generated defects in the bulk are annihilated in a relatively short time without the electrical stress at high temperature.

To further investigate the V_{th} shift phenomenon by the AC pulsed gate and drain bias stress, the effects of V_{ds} voltage, frequency (f), and duty cycle (t_{on}/t_{frame}) are examined with the stress time. Fig. 12(a) shows that the V_{th} shifts more negatively with the stress time as the V_{ds} voltage increases when V_{gs} = −5 V to +15 V, f = 120 Hz, duty cycle = 0.046%, and T = 70 °C are used. The V_{th}

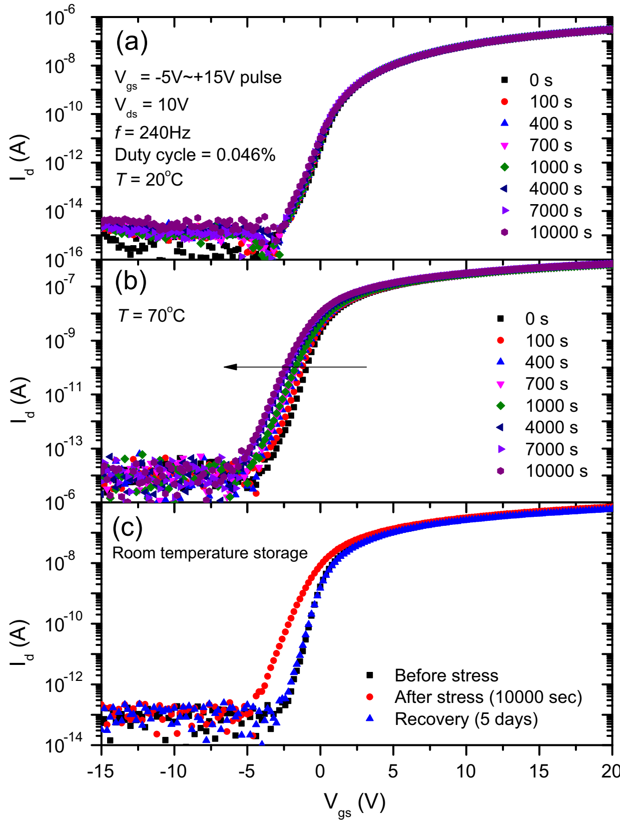


Fig. 11. An example of typical average TFT transfer curve shift with the stress time (a) at 20 °C and (b) 70 °C, and (c) recovery behavior of TFT characteristics after an extended storage at room temperature.

changes (ΔV_{th}) with the stress time are well fitted by the stretched exponential equation [35],

$$\Delta V_{th} = \Delta V_0 \left\{ 1 - \exp\left[-\left(\frac{t_{st}}{\tau} \right)^{\beta} \right] \right\}, \quad (13)$$

where ΔV_0 is the difference between stress voltage V_{st} (e.g. -5 V) and initial threshold voltage V_{th0} ($\Delta V_0 = V_{st} - V_{th0}$), τ represents the characteristic trapping time of carriers, and β is the stretched-exponential exponent. The extracted stretched exponential parameters (τ and β), for the stress conditions used in this study, are listed in Table 3. The stretched-exponential time dependence of ΔV_{th} can be associated with the trapping of charges into the existing traps and/or the continuous redistribution of charges located in the gate dielectric or at the channel/dielectric interface [30,35]. The V_{ds} voltage dependence of ΔV_{th} can be explained by the electron–hole or positively charged species pairs generation at the drain side by impact ionization that is accelerated by high drain-to-source lateral electrical field and high temperature. The electron and positively charged species pairs are generated in the very short period of V_{gs} = +15 V under positive V_{ds}. The existence of increasing self-heating in the channel with the stress time and drain bias stress caused by the drain current have already been established by the thermal analysis [36–38]. The oxygen vacancies (V_o^{2+}) are possible candidates of positively charged species [39,40]. The generated electrons are swept into the drain electrode by the positive drain voltage, but positively charged species are attracted and then trapped near the channel/gate dielectric interface in the period of V_{gs} = -5 V which takes most of the time (t_{off} = 8.33 ms ≈ t_{frame}) during each frame except for a very short positive pulse (e.g. at UHD 120 Hz, t_{on} = 3.9 μs). Therefore the stretched-exponential modeling with V_{st} = -5 V is appropriate. The average transfer curve at V_{ds} = 0 V (e.g. no impact ionization) also shifts to

Table 3
The stretched exponential parameters for various stress conditions used for calculation of the curve fits shown in Fig. 12.

		τ (s)	β
V_{ds} (V)	0	2×10^7	0.34
	5	8×10^5	0.43
	10	3×10^5	0.48
Frequency (Hz)	60	5×10^5	0.43
	120	3×10^5	0.48
	240	2×10^5	0.49
Duty cycle (%)	0.046	3×10^5	0.48
	10	6×10^5	0.30
	50 at V_{ds} = 0 V	9×10^6	0.56

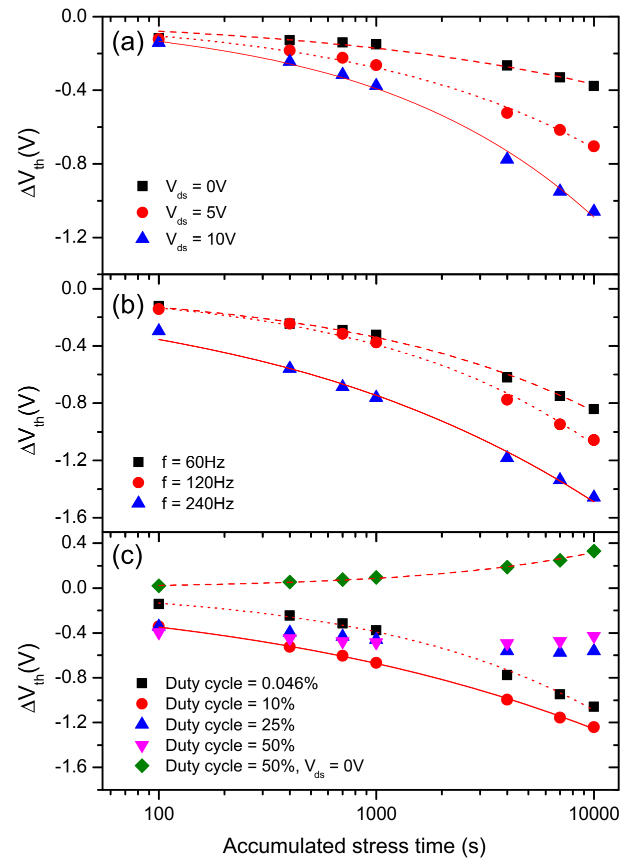


Fig. 12. The V_{th} evolution with the accumulated stress time for different (a) V_{ds} stress voltage, (b) frequency (f), and (c) duty cycle (t_{on}/t_{frame}). The AC BTS temperature was maintained at 70 °C. Stretched exponential fitting parameters are summarized in Table 3.

the direction of negative bias, but this is only due to pulsed AC gate bias without supplying additional trapping charges at the channel/-gate dielectric interface. We speculate that the V_{th} shift is mainly attributed to the charge trapping and can be well described by stretched-exponential model. The nearly full recovery of TFT characteristics to their initial state with negligible degradation of sub-threshold swing at high temperature which may be caused by the positively charged species generated in the bulk by the impact ionization supports this speculation.

To examine the influence of the number of turn-on per one gate line [N_{on} = frequency (f) × accumulated stress time in s (t_{st})] and length of turn-on time during a given stress time (t_{st}) on the impact ionization, the effects of frequency and duty cycle on ΔV_{th} were investigated. Since high frame-rate devices (e.g. 240 Hz) have very short turn-on time (e.g. ~1.9 μs), it needs to be checked whether

such a short time is sufficient to induce the impact ionization during the drain bias. On the other hand, if the turn-on time is extended at the same refresh rate, the influence of positive gate bias during the pulsed gate stress cannot be ignored in attracting the electrons generated by the impact ionization. As the frequency increases from 60 Hz to 240 Hz, the turn-on time (t_{on}) per a frame decreases from 7.7 μs to 1.9 μs but the number of turn-on increases from 6×10^5 to 24×10^5 during the stress time of 10,000 s. Fig. 12(b) shows that as the frequency increases, the magnitude of ΔV_{th} increases when $V_{gs} = -5$ V to +15 V, $V_{ds} = 10$ V, duty cycle = 0.046%, and $T = 70$ °C are used for AC BTS. It was found that even a short turn-on time of 1.9 μs at 240 Hz is sufficient to generate the electron–hole (or positively charged species) pairs by the impact ionization. These results are consistent with Chen et al.'s report [41]; in their study turn-on time varied from 1 μs to 100 μs and the ΔV_{th} s were independent of turn-on time in the investigated range. Therefore, the negative shift of threshold voltage during AC bias-temperature stress should be carefully considered to realize a high frame-rate driving in UHD AM-LCDs.

Fig. 12(c) shows the effect of duty cycle on the ΔV_{th} for $V_{gs} = -5$ V to +15 V, $V_{ds} = 10$ V, $f = 120$ Hz, and $T = 70$ °C AC BTS conditions. The increment of duty cycle at the same refresh rate can show the effect of extended positive gate bias on the electron and/or positively charged species trapping. The ΔV_{th} shifts more negatively for duty cycle of 10% in comparison to 0.046%. This can be attributed to the generation of larger number of electron–hole (positively charged species) pairs over the extended period of time, *e.g.* from 3.9 μs to 0.83 ms at UHD 120 Hz, and/or the hole trapping at the channel/gate dielectric interface induced by a longer negative gate bias. However, when the duty cycle increases up to 25% and 50%, the ΔV_{th} first shifts negatively but eventually turns to the positive direction after 4000 s. This behavior can be associated with the competitive processes between the electron trapping by a positive gate bias during an extended turn-on time and trapping of more positively charged species generated by the impact ionization during a corresponding turn-on time. When the same stress condition of 50% duty cycle is applied at $V_{ds} = 0$ V, the ΔV_{th} shifts positively as shown in Fig. 12(c) due to larger positive gate bias stress during AC gate pulse (V_{GH} +15 V > V_{GL} −5 V). These results clearly indicate the important role of drain bias stress in generating the electron–hole pairs needed for the hole trapping at the channel/gate dielectric interface.

Long channel a-IGZO TFTs have also been exhibiting the asymmetrical degradation behavior between source and drain electrodes due to the different stress voltage and temperature distribution [37,38,40,42–44]. This asymmetrical degradation between source and drain electrodes can be simply checked by confirming the difference between the forward mode and reverse mode of transfer curve before and after stress [44–46]. The forward mode of transfer curve is defined when the source-drain electrodes remain in the same position as that of the stressed condition and the reverse mode is defined when the source-drain electrodes are interchanged with respect to stressed condition. The forward and reverse mode of transfer curve of TFT arrays used in this study does not show any differences before and after stress (not shown). This symmetrical degradation behavior between source and drain electrodes is mainly associated with the charge trapping of holes which are relatively uniformly distributed in the short channel devices. Also, the temperature is more evenly distributed in short channel in comparison to long channel TFTs [38].

4. Conclusions

In this work, the electrical characteristics and stability of the ultra-high definition a-IGZO TFT arrays were examined. Compared to the long channel length TFTs, the a-IGZO TFT arrays electrical characteristics showed short channel effects. The non-saturation of output curve at high V_{ds} was explained by the channel length modulation caused by effective channel length reduction as the channel length decreases. The negative shift of threshold voltage in the average transfer curve with the increasing V_{ds} was observed and is described by the drain-induced-barrier lowering (DIBL). To obtain robust and physically meaningful threshold voltage, the second derivative method adopting Tikhonov's regularization theory was introduced and compared with the other V_{th} extraction methods. The difference between the I_d experimental and fitted data as a function of V_{gs} was considered as the reduction of effective gate voltage by the source/drain contact resistances. The mobility reduction at high V_{gs} is also believed to be associated with the source/drain contact resistances influence as the channel length decreases. The extracted γ values showed only slight temperature dependency by taking into consideration the impact of source/drain contact resistances. To simulate the actual operation of AM-LCDs, the AC bias-temperature stress stability of TFT arrays was investigated. The V_{th} has a dependency on the magnitude of drain bias stress, frequency, and duty cycle at high temperature. The main mechanism responsible for threshold voltage shift appears to be associated with the hole trapping at the channel/gate dielectric interface over long negative gate-biased time; the electron–hole (positively charged species) pairs generated by the thermally accelerated impact ionization are at the origin of holes creation. This study showed that the electrical characteristics and stability of the UHD a-IGZO TFT arrays to be used for high frame-rate high-end displays should be thoroughly investigated. The short channel effects, source/drain contact resistances and impact ionization should be taken into consideration when optimization of pixel design for future UHD displays is performed.

Acknowledgment

This research was supported at the University of Michigan by Samsung Display Co., Ltd. under the Visiting Scholar Program 2014.

References

[1] Nomura K, Ohta H, Takagi A, Kamiya T, Hirano M, Hosono H. Room-temperature fabrication of transparent flexible thin-film transistors using amorphous oxide semiconductors. Nature 2004;432:488–92.
[2] Park JS, Maeng WJ, Kim HS, Park JS. Review of recent developments in amorphous oxide semiconductor thin-film transistor devices. Thin Solid Films 2012;520:1679–93.
[3] Park JS, Kim H, Kim ID. Overview of electroceramic materials for oxide semiconductor thin film transistors. J Electroceram 2014;32:117–40.
[4] Lu HH, Ting HC, Shih TH, Chen CY, Chuang CS, Lin Y. 32-inch LCD panel using amorphous indium–gallium–zinc–oxide TFTs. In: SID symp int tech papers; 2010. p. 1136–1139.
[5] Song J, Lim JH, Ahn BD, Lee J. High mobility oxide TFTs for future LCD applications. In: SID Symp Int Tech Papers; 2013. p. 93−96.
[6] Park JS. Oxide TFTs for AMOLED TVs. Inf Disp 2013;29:16–9.
[7] http://www.samsunghub.com/2010/11/08/samsung-develops-70-inch-lcd-panel-using-oxide-semiconductor-tech/.
[8] Heo YW, Cho KM, Sun SY, Kim SY, Lee JH, Kim JJ, et al. Effects of channel dimensions on performance of a-InGaZnO$_4$ thin-film transistors. J Vac Sci Technol, B 2011;29:021203.1–3.7.
[9] Cho EN, Kang JH, Yun I. Contact resistance dependent scaling-down behavior of amorphous InGaZnO thin-film transistors. Curr Appl Phys 2011;11:1015–9.
[10] Park JS. Characteristics of short-channel amorphous In–Ga–Zn–O thin film transistors and their circuit performance as a load inverter. J Electroceram 2012;28:74–9.
[11] Kang DH, Han JU, Mativenga M, Ha SH, Jang J. Threshold voltage dependence on channel length in amorphous–indium–gallium–zincoxide thin-film transistors. Appl Phys Lett 2013;102:083508.1–8.4.
[12] Ha SH, Kang DH, Kang I, Han JU, Mativenga M, Jang J. Channel length dependent bias-stability of self-aligned coplanar a-IGZO TFTs. J Disp Technol 2013;9:985–8.

[13] Cho IT, Lee JM, Lee JH, Kwon HI. Charge trapping and detrapping characteristics in amorphous InGaZnO TFTs under static and dynamic stresses. Semicond Sci Technol 2009;24:015013.1–3.6.

[14] Kim SJ, Lee YW, Lee SY, Woo JS, Kwon JY, Han MK, et al. The effect of AC bias frequency on threshold voltage shift of the amorphous oxide TFTs. In: SID Symp Int Tech Papers; 2011. p. 1195–1197.

[15] Chen TC, Chang TC, Hsieh TY, Lu WS, Jian FY, Tsai CT, et al. Investigating the degradation behavior caused by charge trapping effect under DC and AC gate-bias stress for InGaZnO thin film transistor. Appl Phys Lett 2011; 99:022104.1–4.3.

[16] Yang CY, Huang SC, Chiu HL, Hsieh T, Yeh BL, Lin CS, et al. AC gate-drain-bias stress study of amorphous indium gallium zinc oxide thin film transistors for GOA applications. In: SID Symp Int Tech Papers; 2012. p. 1126–1128.

[17] Kim SJ, Lee SY, Lee YW, Kuk SH, Kwon JY, Han MK. Effect of charge trapping/detrapping on threshold voltage shift of IGZO TFTs under AC bias stress. Electrochem Solid State Lett 2012;15(4):H108–10.

[18] Yu EKH, Abe K, Kumomi H, Kanicki J. AC bias-temperature stability of a-InGaZnO thin-film transistors with metal source/drain recessed electrodes. IEEE Trans Electron Devices 2014;61(3):806–12.

[19] Wie CR. Nonsaturating drain current characteristic in short-channel amorphous–silicon thin-film transistors. IEEE Trans Electron Devices 2010;57(4):846–54.

[20] Fortunato G, Valletta A, Gaucci P, Mariucci L, Brotherton SD. Short channel effects in polysilicon thin film transistors. Thin Solid Films 2005;487:221–6.

[21] Smith KC, Sedra AS. Microelectronic circuits. New York: Oxford University Press; 2004.

[22] Kanicki J, Martin S. Hydrogenated amorphous silicon thin-film transistors. In: Kagan CR, Andry P, editors. Thin-film transistors. New York: Dekker; 2003. p. 71–137.

[23] Chen C, Abe K, Kumomi H, Kanicki J. Density of states of a-InGaZnO from temperature-dependent field-effect studies. IEEE Trans Electron Devices 2009;56(6):1177–82.

[24] Taur Y, Ning TH. Fundamentals of modern VLSI devices. Cambridge: Cambridge University Press; 1998.

[25] Baek G, Abe K, Kumomi H, Kanicki J. Scaling of a-InGaZnO TFTs and pixel electrode for AM-LCDs. In: AM-FPD 19th int workshop; 2012. p. 13–16.

[26] Wong HS, White MH, Krutsick TJ, Booth RV. Modeling of transconductance degradation and extraction of threshold voltage in thin oxide MOSFETs. Solid State Electron 1987;30(9):953–68.

[27] Booth RV, White MH, Wong HS, Krutsick TJ. The effect of channel implants on MOS transistor characterization. IEEE Trans Electron Devices 1987;ED-34:2501–9.

[28] He J, Xi X, Chan M, Cao K, Hu C, Li Y, et al. Normalized mutual integral difference method to extract threshold voltage of MOSFETs. IEEE Electron Device Lett 2002;23:428–30.

[29] Choi WY, Kim H, Lee B, Lee JD, Park BG. Stable threshold voltage extraction using Tikhonov's regularization theory. IEEE Trans Electron Device 2004;51(11):1833–8.

[30] Fung TC, Abe K, Kumomi H, Kanicki J. Electrical instability of RF sputter amorphous In–Ga–Zn–O thin-film transistors. J Disp Technol 2009; 5(12):452–61.

[31] Kim SC, Kim YS, Kanicki J. Density of states of short channel amorphous InGaZnO TFT arrays fabricated using manufacturable processes. Jpn J Appl Phys 2015;54(5):051101.1–1.7.

[32] Kuo A. High performance hydrogenated amorphous thin-film transistor structure. University of Michigan Ph.D. dissertation; 1997, p. 121.

[33] Kishida S, Naruke Y, Uchida Y, Matsumura M. Theoretical analysis of amorphous-silicon field-effect-transistors. Jpn J Appl Phys 1983;22(3):511–7.

[34] Abe K, Sato A, Takahashi K, Kumomi H, Kamiya Hosono TH. Mobility- and temperature-dependent device model for amorphous In–Ga–Zn–O thin-film transistors. Thin Solid Films 2014;559:40–3.

[35] Libsch FR, Kanicki J. Bias-stress-induced stretched-exponential time dependence of charge injection and trapping in amorphous thin-film transistors. Appl Phys Lett 1993;62:1286–8.

[36] Fujii M, Uraoka Y, Fuyuki T, Jung JS, Kwon JY. Experimental and theoretical analysis of degradation in Ga_2O_3–In_2O_3–ZnO thin-film transistors. Jpn J Appl Phys 2009;48. 04C091.1–1.6.

[37] Urakawa S, Tomai S, Ueoka Yamazaki YH, Kasami M, Yano K, Wang D, et al. Thermal analysis of amorphous oxide thin-film transistor degraded by combination of joule heating and hot carrier effect. Appl Phys Lett 2013;102:053506.1–6.4.

[38] Kim JI, Chang KS, Kim DU, Cho IT, Jeong CY, Lee D, et al. Thermoreflectance microscopy analysis on self-heating effect of short-channel amorphous In–Ga–Zn–O thin film transistors. Appl Phys Lett 2014;105:043501.1–1.4.

[39] Oh H, Hwang CS, Pi JE, Ryu MK, Park SHK, Chu HY. Unusual instability mode of transparent all oxide thin film transistor under dynamic bias condition. Appl Phys Lett 2013;103:123501.1–1.5.

[40] Lee D, Jeong CY, Song SH, Xiao-Shi J, Kim JI, Lee JH, et al. Asymmetrical degradation behaviors in amorphous InGaZnO thin-film transistors under various gate and drain bias stresses. J Vac Sci Technol, B 2015;33(1):011202.1–2.8.

[41] Chen TC, Chang TC, Hsieh TY, Tsai MY, Chen YT, Chung YC, et al. Self-heating enhanced charge trapping effect for InGaZnO thin film transistor. Appl Phys Lett 2012;101:042101.1–1.4.

[42] Hsieh TY, Chang TC, Chen TC, Tsai MY, Chen YT, Chung YC, et al. Origin of self-heating effect induced asymmetrical degradation behavior in InGaZnO thin-film transistors. Appl Phys Lett 2012;100:232101.1–1.4.

[43] Hsieh TY, Chang TC, Chen TC, Tsai MY, Chen YT, Jian FY, et al. Investigating the drain-bias-induced degradation behavior under light illumination for InGaZnO thin-film transistors. IEEE Electron Dev Lett 2012;33(7):1000–2.

[44] Seo SB, Park HS, Jeon JH, Choe HH, Seo JH, Yang S, et al. Drain bias effect on the instability of amorphous indium gallium zinc oxide thin film transistor. Thin Solid Films 2013;547:263–6.

[45] Dey A, Allee DR, Clark LT. Impact of drain bias stress on forward/reverse mode operation of amorphous ZIO TFTs. Solid State Electron 2011;62:19–24.

[46] Jeong CY, Lee D, Song SH, Kim JI, Lee JH, Kwon HI. A study on the degradation mechanism of InGaZnO thin-film transistors under simultaneous gate and drain bias stresses based on the electronic trap characterization. Semicond Sci Technol 2014;29:045023.1–3.6.